

VLSI Photonics
Common Optical Module
Final DARPA Review
30 July 2001

Component Development Objectives

Prior Demo

During VLSI Photonics Pgm.

Future

<p><u>OPTOMECHANICS</u></p> <p><i>CONNECTOR</i> Bulk ✓ Machined/baseplate ✓</p> <p><i>MEDIUM</i> Air ✓ Rigid cascable ✓</p>		<p>Machined/clickfit ✓</p> <p>Image Guide ✓</p> <p>2-D Fiber Bundle ✓</p>		<p>IMP/clickfit ✓</p> <p>Optical/Ribbon ✓</p>		<p>One-piece assembly</p>	
<p><u>ELECTRONICS</u></p> <p><i>VOLTAGE</i> 5 - 10 V ✓</p> <p><i>CIRCUITRY</i> None ✓ Tx/Rx ✓</p> <p><i>BIT RATE/CHAN (for Array)</i> 40Mb/s ✓</p>		<p>3 - 5V ✓</p> <p>Addressing ✓</p> <p>200Mb/s ✓</p> <p>.35 CMOS ✓</p>		<p>1.8 - 2.5V ✓</p> <p>Buffer ✓</p> <p>1 Gb/s ✓</p> <p>.25 CMOS ✓</p>		<p>Error Correct 2 bit</p> <p>Threshold control</p> <p>Error Correct 1 bit ✓</p> <p>10 Gb/s ✓</p> <p>.18 CMOS ✓</p>	<p>.9 - 1.2 V</p> <p>Full I/O Processor</p> <p>>10Gb/s</p> <p>SiGi / SoS</p>
<p><u>OPTICAL CHIPS (large arrays)</u></p> <p>Modulators ✓</p> <p>RCLEDs ✓</p>		<p>VCSELs</p> <p>16x16 ✓</p> <p>Vt=few mA ✓</p>		<p>64x64 ✓</p> <p>Vt<1mA ✓</p>		<p>128x128</p> <p>Vt< 1mA</p> <p>VCSELs (1.3)</p> <p>Vt < 100µA</p>	
<p><u>PROGRAM DEMOS</u></p>		<p>1 ✓</p> <p>1.5 ✓</p>		<p>2 3</p>			

Year 95 96 97 98 99 00 01 02 05



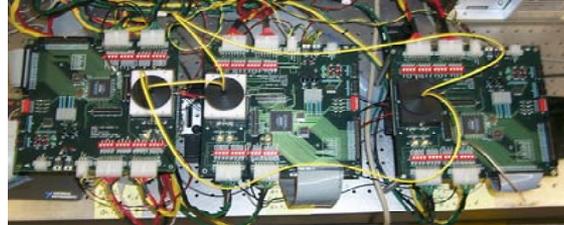
VLSI Photonics progress

Point to Point - Sep. 99

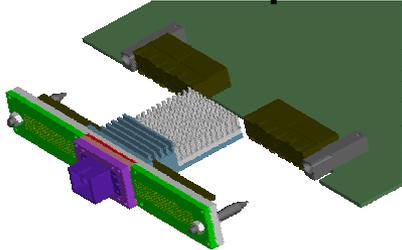


16x16 arrays

3 Board Network- Dec. 99

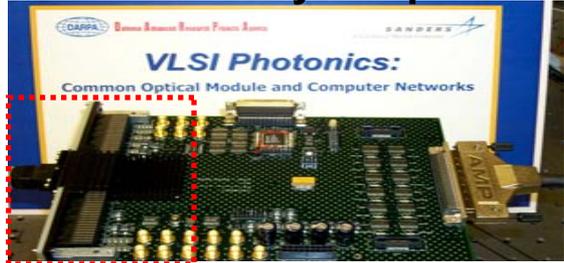


Module Concept - Feb. 00

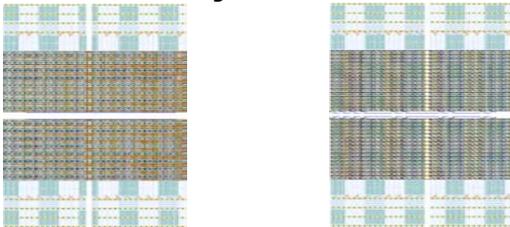


16x20 arrays

Module Reality - Sep. 00

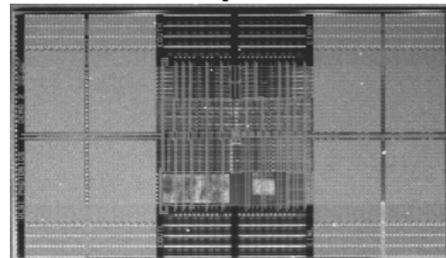


Demo 2 Layout - Nov. 00



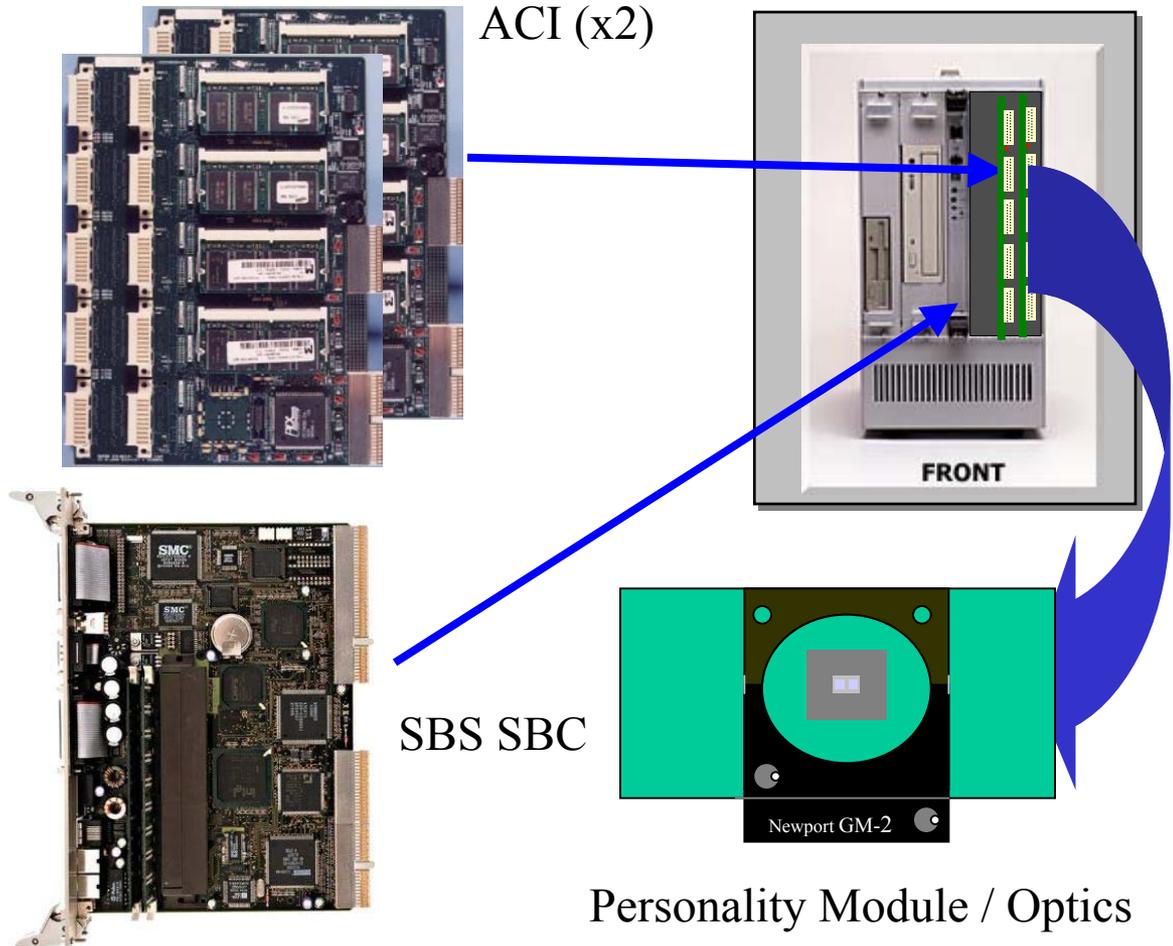
32x34 arrays

Demo 2 Chip - Mar. 01

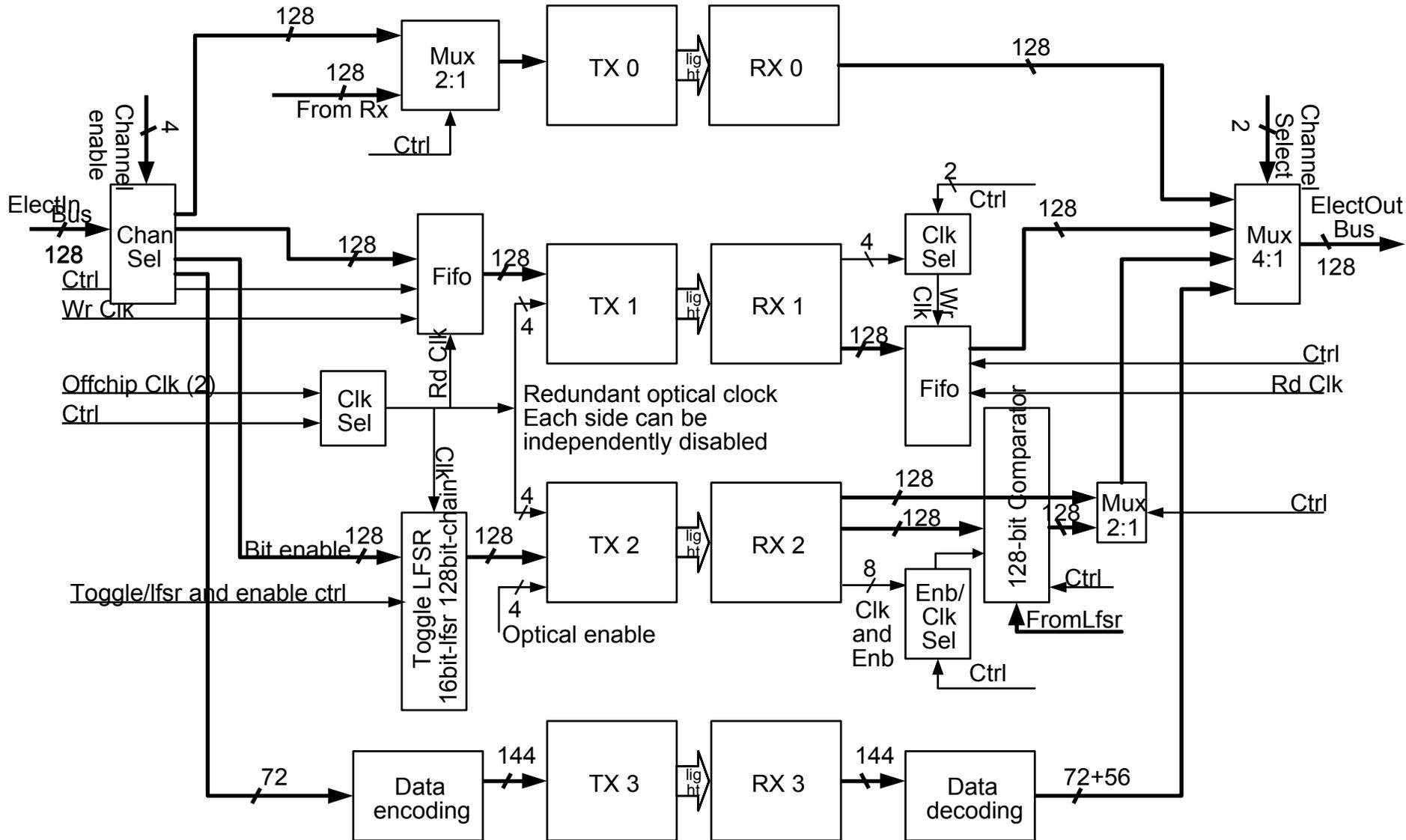


Demo 2 Hardware

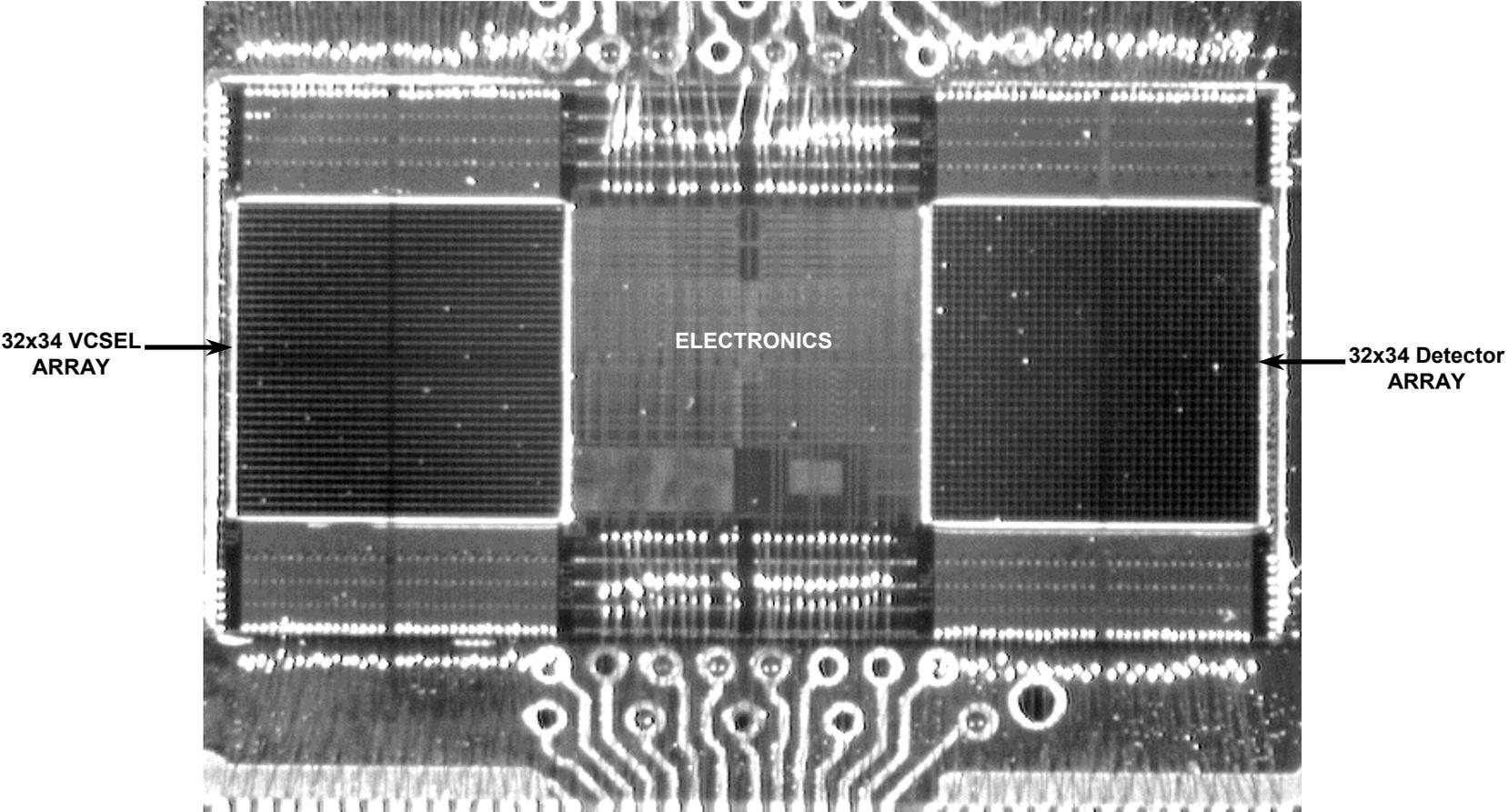
- Demonstration system
 - Optical module
 - Demo2 chip
 - VCSEL/PIN Arrays
 - Silicon Interposer
 - Personality Module
 - ACI - Control Electronics Boards
 - Single Board Computer



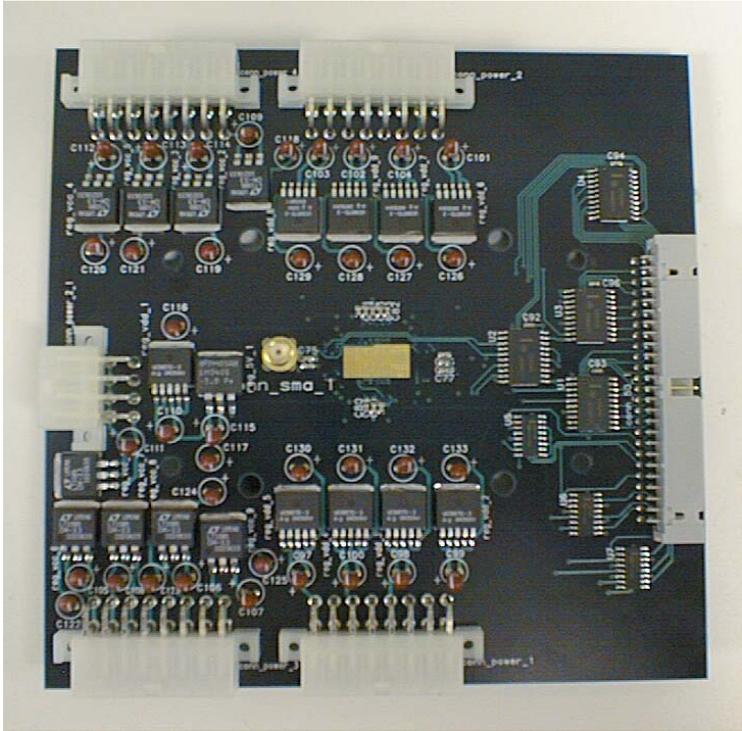
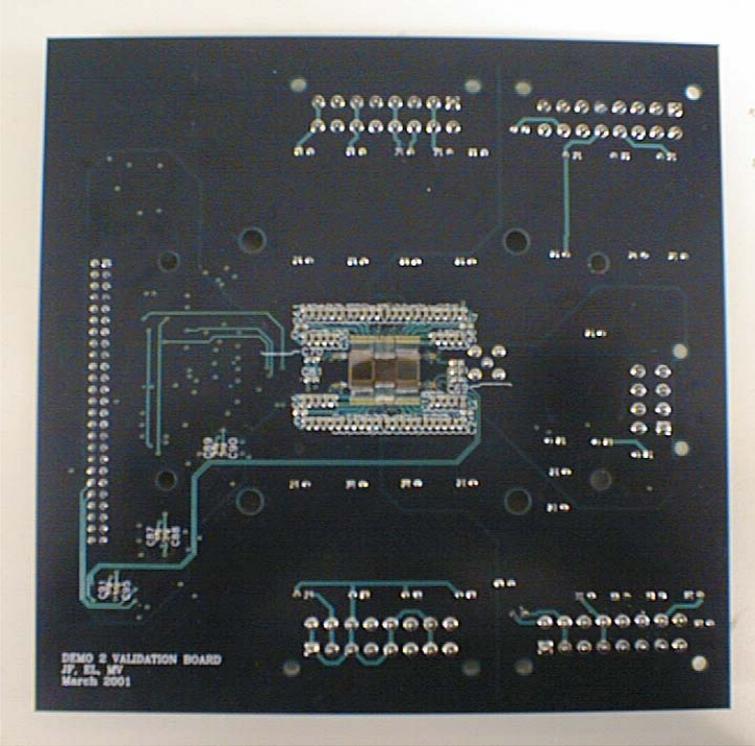
DEMO 2 chip functions



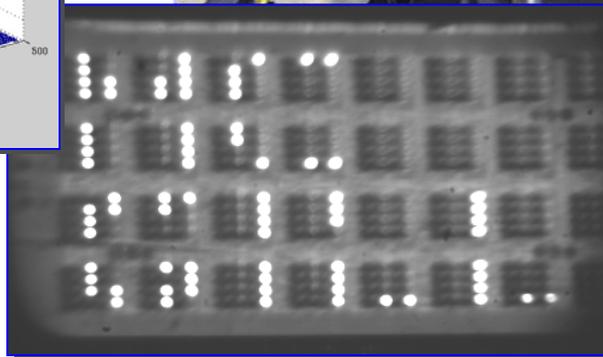
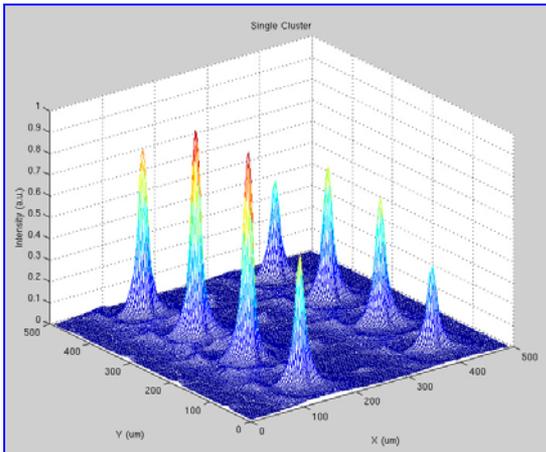
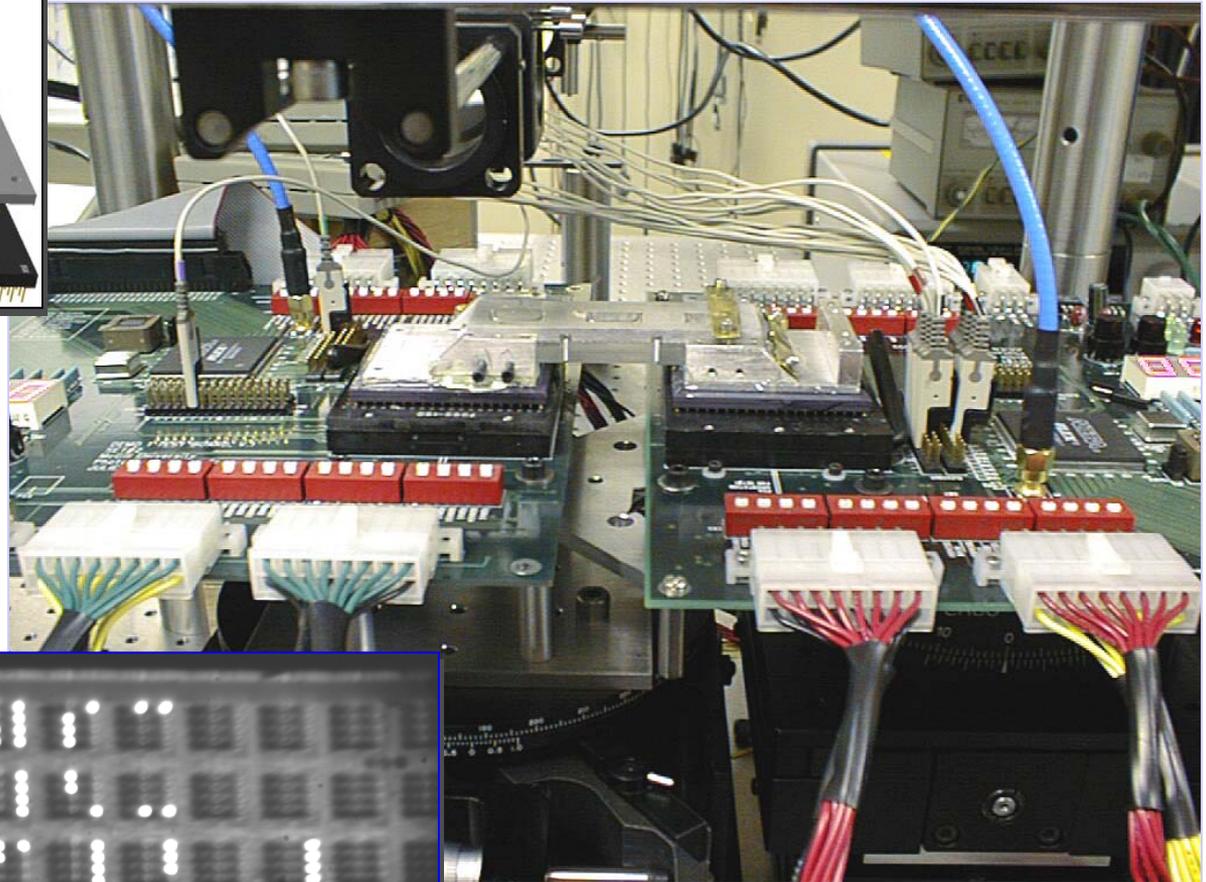
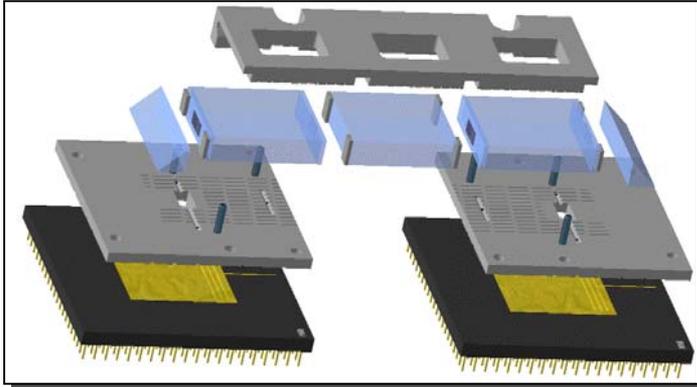
Demo 2 chip with hybridized vcsels and detectors



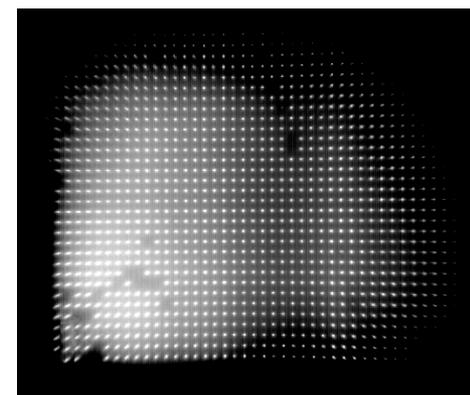
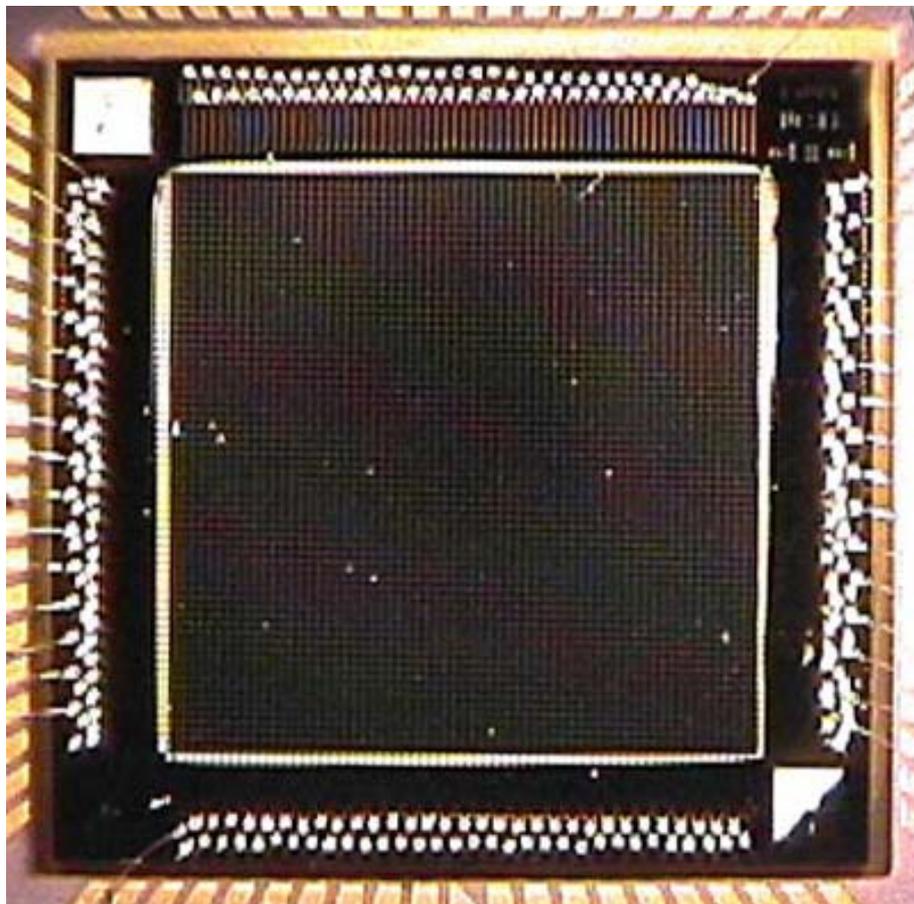
Demo 2 evaluation board



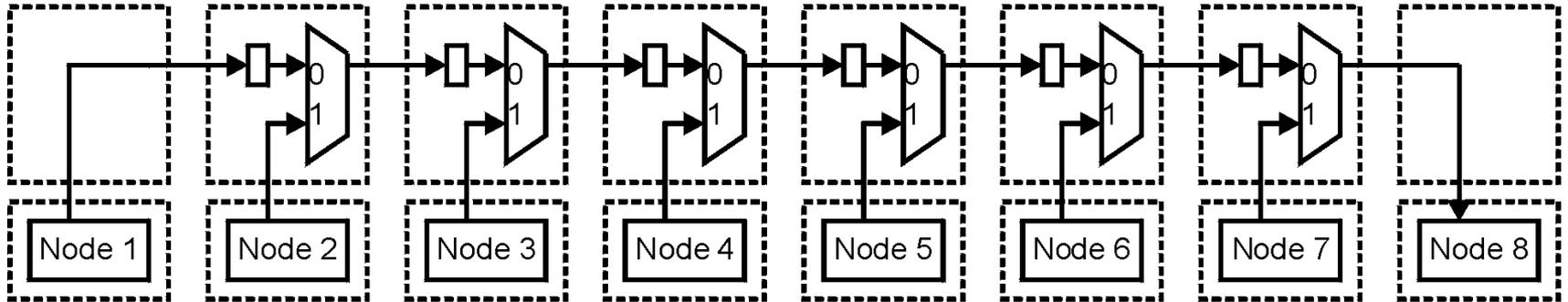
Demo 1.5 Optics



64x64 Array



Reconfigurability in a Multiring

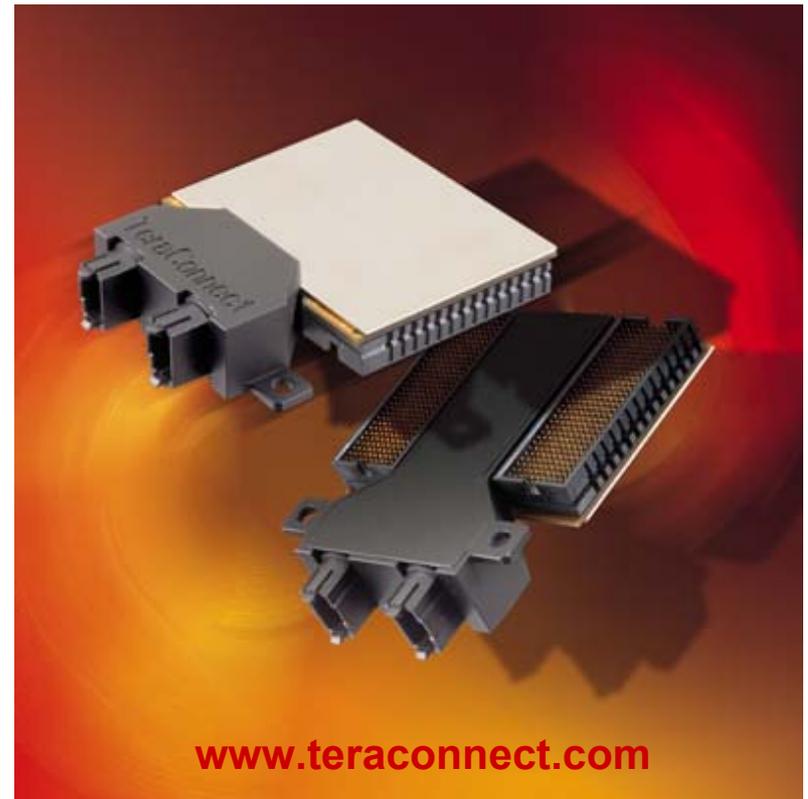


8 node ring

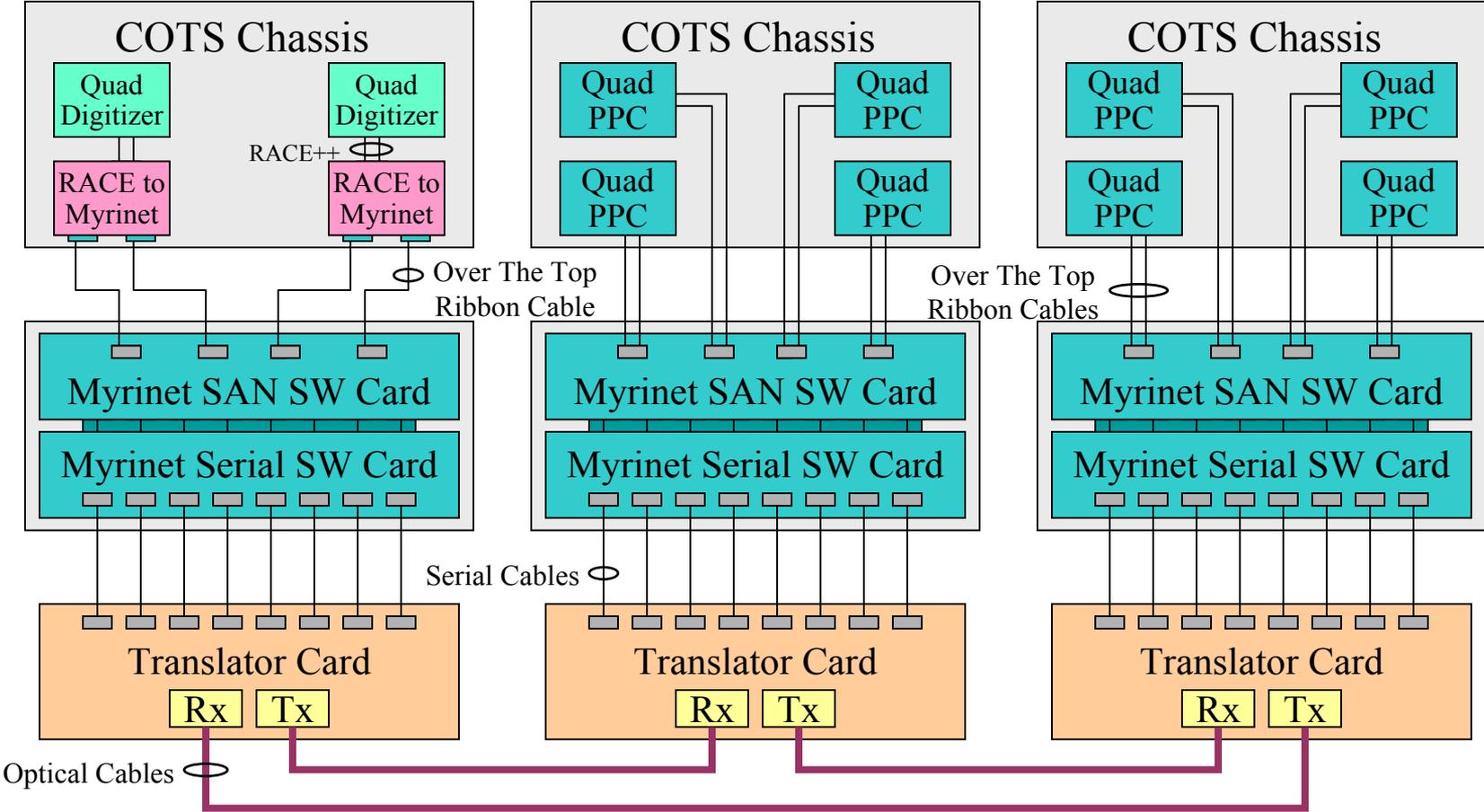
- Bandwidth of subring set by the number of VCSELs/PDs used to establish path
- Relative bandwidth allocation within a subring set by quota within DRR fairness protocol
- Result is fully reconfigurable bandwidth allocation

Commercial spin out (TeraConnect)

- Concept based on VLSI Photonics developments.
- 48 patents transferred.
- Spin out occurred November 2000.
- Initial VC funding \$40M.
- First product (T48) announced May 2001.



Demonstration 3 Configuration



ACCOMPLISHMENTS

- **16X16 ARRAY NETWORK .35 CMOS**
- **16X20 COMMERCIAL TEST CHIP .25 CMOS - INTERCONNECTED WITH ORDERED FIBER ARRAY.**
- **32X34 FOUR FUNCTION TEST CHIP DEVELOPED .25 CMOS.**
- **OPTICAL GLASS BUILDING BLOCK LENS ARCHITECTURE DEMONSTRATED AND TESTED.**
- **64X64 ARRAY FABRICATED**
- **MULTI NODE ARCHITECTURE SIMULATIONS COMPLETED WITH FAIRNESS PROTOCOL TESTED.**
- **TERACONNECT SPIN OUT**

OBJECTIVES

- **128X128 ARRAY IN FABRICATION**
- **INTERCONNECTED TESTING OF DEMO 2 CHIP FUNCTIONS**
- **MILITARY INSERTION DEMONSTRATION USING COTS**